CLAIMS

We claim the following invention:

1. A model that simulates logic signals capable of having more than two unique decimal values and one or more unique drive states, comprising:

a signal value field, said signal value field further comprises information that conveys the decimal value of the logic signal being modeled;

a signal strength field, said signal strength field further comprises information that conveys the drive state of the logic signal being modeled; and

a signal definition field, said signal definition field further comprises information that conveys whether the signal being modeled holds a defined value or an undefined value.

2. The model of Claim 1, wherein said signal value field is capable of holding up to 32 unique decimal signal values.

3. The model of Claim 1, wherein said signal strength field is capable of conveying whether said decimal value of the logic signal being modeled is in the, the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

4. The model of Claim 3, wherein said signal strength field conveys that said decimal value of the logic signal being modeled is strongly driven when said signal strength field is set to "00".

5. The model of Claim 1, wherein said signal definition field holds the value of "0" when said logic signal being modeled is a valid, defined signal.

6. A method that models logic signals capable of having more than two unique decimal values and one or more unique drive states for use in simulation, comprising:

defining a signal value field that comprises information that conveys the decimal value of the logic signal being modeled;

defining a signal strength field that comprises information that conveys the drive state of the logic signal being modeled; and

defining a signal definition field that comprises information that conveys whether the signal being modeled holds a defined value or an undefined value.

7. The method of Claim 6, wherein said signal value field is capable of holding up to 32 unique decimal signal values.

8. The method of Claim 6, wherein said signal strength field conveys whether said decimal value of the logic signal being modeled is in the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

9. The method of Claim 8, wherein a value of "00" in said signal strength field conveys that said decimal value of the logic signal being modeled is strongly driven.

10. The method of Claim 6, wherein said signal definition field holds the value of "0" when said logic signal being modeled is a valid, defined signal.

11. A method that uses a logic signal model in a software-implemented simulation of a logic design, wherein said logic signal is capable of having more than two unique decimal values and one or more unique drive states, comprising:

reading a signal value field that comprises information that conveys the decimal value of the logic signal being modeled;

reading a signal strength field that comprises information that conveys the drive state of the logic signal being modeled;

reading a signal definition field that comprises information that conveys whether the signal being modeled holds a defined value or an undefined value; and

providing said decimal value, said drive state, and said definition information of the logic signal being modeled to the software-implemented simulation of the logic design.

12. The method of Claim 11, wherein said signal value field is capable of holding up to 32 unique decimal signal values.

13. The method of Claim 11, wherein said signal strength field conveys whether said decimal value of the logic signal being modeled is in the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

14. The method of Claim 13, wherein a value of "00" in said signal strength field conveys that said decimal value of the logic signal being modeled is strongly driven.

15. The method of Claim 11, wherein said signal definition field holds the value of "0" when said logic signal being modeled is a valid, defined signal.

16. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method that uses a logic signal model in a software-implemented simulation of a logic design, wherein said logic signal is capable of having more than two unique decimal values and one or more unique drive state, said method comprises:

reading a signal value field that comprises information that conveys the decimal value of the logic signal being modeled;

reading a signal strength field that comprises information that conveys the drive state of the logic signal being modeled;

reading a signal definition field that comprises information that conveys whether the signal being modeled holds a defined value or an undefined value; and

providing said decimal value, said drive state, and said definition information of the logic signal being modeled to the software-implemented simulation of the logic design.

17. The program storage device of Claim 16, wherein said signal value field is capable of holding up to 32 unique decimal signal values.

18. The program storage device of Claim 16, wherein said signal strength field conveys whether said decimal value of the logic signal being modeled is in the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

19. The program storage device of Claim 18, wherein a value of "00" in said signal strength field conveys that said decimal value of the logic signal being modeled is strongly driven.

20. The program storage device of Claim 16, wherein said signal definition field holds the value of "0" when said logic signal being modeled is a valid, defined signal.

21. A system that models logic signals capable of having more than two unique decimal values and one or more unique drive states for use in simulation, comprising:

encoding the decimal value of the logic signal being modeled in a signal value field;

encoding the drive state of the logic signal being modeled in a signal strength field; and

encoding whether the signal being modeled holds a defined value or an undefined value in a signal definition field.

22. The system of Claim 21, wherein said signal value field is capable of holding up to 32 unique decimal signal values.

23. The system of Claim 21, wherein the drive state encoded in said signal strength field indicates whether said decimal value of the logic signal being modeled is in the high-impedance state, the

weakly-driven state, the moderately-driven state, or the strongly-driven state.

24. The system of Claim 23, wherein a value of "00" encoded in said signal strength field indicates that said decimal value of the logic signal being modeled is strongly driven.

25. The system of Claim 21, wherein a value of "0" in said signal definition field indicates that said logic signal being modeled is a valid, defined signal.